REMARKS

Claims 16-23 are currently pending in the application. By this amendment claim 18 is amended, and replacement Figures 1-4 are provided for the Examiner's consideration. Reconsideration of the rejected claims in view of the above amendments and the following remarks is respectfully requested.

Objection to Drawings

The drawings were objected to for informalities. For example, Figure 1 was objected to for lack of a legend, and Figures 1-4 were objected for being informal. By this Amendment, replacement Figures 1-4 are provided. Replacement Figure 1 is a formal drawing having the requested legend. Figures 2-4 are drawings having the informalities removed. No new matter is added. Accordingly, Applicants respectfully request that the drawing objection be withdrawn.

Objection to Claims

Claim 18 was objected to for informalities. In particular, claim 18 was objected to for the use of the term of "forming." Claim 18 has been amended to replace the term "forming" with the term "selecting." Accordingly, Applicants respectfully request that the objection to claim 18 be withdrawn.

35 U.S.C. §102 Rejection

AAPA

Claims 16-23 were rejected under 35 U.S.C. §102(b) for being anticipated by Applicants' Admitted Prior Art (AAPA). This rejection is respectfully traversed.

The invention relates to hyper-abrupt (HA) junction varactors and to a simplified method of fabrication of HA junction varactors. The invention simplifies varactor fabrication and tightens manufacturing tolerances by eliminating one or more etching or layer formation steps.

The varactor formation process of the invention reduces or avoids etching or layer formation steps by relying mostly on doping steps to form the active region of the varactor. This process and resulting structure is less expensive and easier to produce with tighter manufacturing tolerances. Other advantages include easily altering the C-V tuning by adjusting the doping rates. Thus, C-V tuning curves are shown to be within design parameters using the invention. The invention is compatible with complex fabrication processes or complex circuitry. In fact, the design of the invention uses a semiconductor substrate without little or no etching, or the like, required.

The AAPA shows a varactor 10 having a silicon (Si) substrate 12 with a low temperature epitaxy (LTE) layer 26 formed thereupon. The LTE layer 26 is formed by a low temperature epitaxial formation process where additional material is formed upon the surface of the Si substrate. Accordingly, the AAPA shows a Si substrate 12 having an N+ subcollector 14 formed by a doping process. The collector formation, as noted in the background section, is formed by a unique implant step, unlike the present invention in which the collector is formed by the tail of the deep implant process.

The hyper-abrupt junction layer 24 is formed by a doping process of the Si substrate 12. After the upper layer of the Si substrate 12 is doped to form the hyper-abrupt junction layer 24, an additional layer is added to the top of the Si substrate 12 to form the LTE layer 26. Accordingly, the structure of the varactor 10 includes a Si substrate 12 having doped regions therein upon which an additional layer, i.e., the LTE layer 26 is formed.

Because the AAPA shows a semiconductor substrate with an LTE layer formed thereupon, the AAPA fails to show a method of fabricating a varactor including providing a semiconductor substrate and doping a lower region of the semiconductor substrate with a first dopant, doping a middle region of a semiconductor substrate with a second dopant, and doping an upper region of the semiconductor substrate with a third dopant, as set forth in claim 16.

The Examiner asserts that the AAPA discloses a method of fabricating a varactor, including providing a semiconductor substrate having layers 12 and 26 which can naturally be regarded as a substrate for layer 34 thereupon. However, as discussed above, embodiments of the invention include doping a single substrate to form a lower doped region, a middle doped region, and an upper doped region, i.e.: no additional layer need be added to the top of the substrate. Consequently, embodiments of the invention distinguish over the AAPA because the AAPA requires the addition of an extra layer after doping a lower and middle region and then doping the extra layer to form an upper doped region.

Accordingly, claim 16 is in allowable condition. Claims 17-23 are in allowable condition at least for the reasons discussed above with respect to claim 16, from which they depend, as well as for their added features. Applicants respectfully request the rejection of claims 16-23 be withdrawn.

Kajimura

The office action rejects claims 16-20 under 35 U.S.C. §102(b) for being anticipated by Japanese Patent No. 4-629772 to Kajimura ("Kajimura"). This rejection is respectfully traversed.

Kajimura shows a varactor diode manufacturing process directed to increasing a break-down voltage and increasing the capacity wherein a low resistance layer of an opposite conductivity type is formed on the surface of a layer of a conductivity type so as to be shallower and wider than the layer with both ends protruding to the outside of the action layer.

Referring to Figure d of Kajimura, a layer 6 is formed on top of an action layer 5 where an action layer 5 is a hyper-abrupt n-type action layer. Because action layer 5 is an n-type layer,

it receives an n-type doping. Because layer 6 is a p+ type low-resistance layer, it receives a p+ type doping. Kajimura does not show or suggest any other doping step, and thus there are a total of two doping steps shown in Kajimura.

The Examiner asserts that Kajimura shows a method of fabricating a varactor including doping a middle region and doping an upper region of a semiconductor substrate. However, Kajimura actually shows doping an action layer with an n-type dopant and doping a p+ layer with a p+ type dopant, for a total of two doping steps. Because Kajimura shows only two doping steps, it fails to show a method of fabricating a varactor, including doping a lower region of a semiconductor substrate with a first dopant, doping a middle region of the semiconductor substrate with a second dopant, and doping an upper region of the semiconductor substrate with a third dopant, as set forth in claim 16.

Accordingly, claim 16 distinguishes over Kajimura and should be in allowable condition. Claims 17-20 are allowable over Kajimura at least for the reasons discussed above with respect to independent claim 16, from which they depend, as well as for their additional features. Applicants respectfully request that the rejection of claims 16-20 be withdrawn.

35 U.S.C. §103 Rejection

Claims 21-23 were rejected under 35 U.S.C. §103(a) for being unpatentable over Kajimura. This rejection is respectfully traversed.

The Examiner asserts that Kajimura does not expressly disclose forming an isolation region, a reach-through implant, and/or a silicide layer. The Examiner is of the opinion that one of ordinary skill in the art would readily recognize such steps are common and it would have been obvious to one of ordinary skill in the art to incorporate such steps into the method of Kajimura, such as, for example, in the AAPA. However, as discussed above, claim 16 distinguishes over Kajimura, because Kajimura shows only two doping steps. Accordingly, claims 21-23 are allowable at least for the reasons discussed above with respect to claim 16, from which they depend, as well as for their additional features.

Regarding claim 21, Applicants note that Kajimura shows a thermal oxide film 3 positioned above the p+ type layer 6. Additionally, the AAPA shown in Figure 1 shows an isolation region 18 formed next to the hyper-abrupt junction layer 24, but below the LTE layer 26. Thus claim 21, which sets forth forming at least one isolation region adjacent to a lower, middle, and upper regions of the semiconductor substrate distinguishes over Kajimura.

Regarding claim 23, a process of forming a silicide layer on top of the semiconductor substrate above the upper region is set forth. Kajimura does not shows a silicide layer and the Figure of the AAPA shows a silicided layer 34 formed on top of the LTE layer 26 (rather than the substrate). Consequently, a silicide layer is not formed on top of the semiconductor substrate, as set forth in claim 23. Accordingly, for the reasons discussed above, claims 21-23 distinguish over Kajimura and the APA either alone or in combination, and Applicants respectfully request that the rejection of claims 21-23 be withdrawn.

CONCLUSION

In view of the foregoing amendments and remarks, Applicants submits that all of the claims are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue. The Examiner is invited to contact the undersigned at the telephone number listed below, if needed. Applicants

hereby makes a written conditional petition for extension of time, if required. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 09-0456.

Respectfully submitted,

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REPLACEMENT DRAWINGS

Attached hereto are replacement drawings for Figures 1-4, without any markings. The changes to the drawings are explained below, in the "REMARKS" section. All of the drawings on each replacement sheet, as originally filed, are provided herein. The header of each revised drawing sheet includes the following information: (i) "Replacement Sheet", (ii) application number and (iii) date information. The Examiner is requested to provide an indication of such consideration in the next Office Action.